

Z.A.D.

**Analog
To
Digital
Interface**

for the Timex/Sinclair
ZX81/TS1000/1500/2068

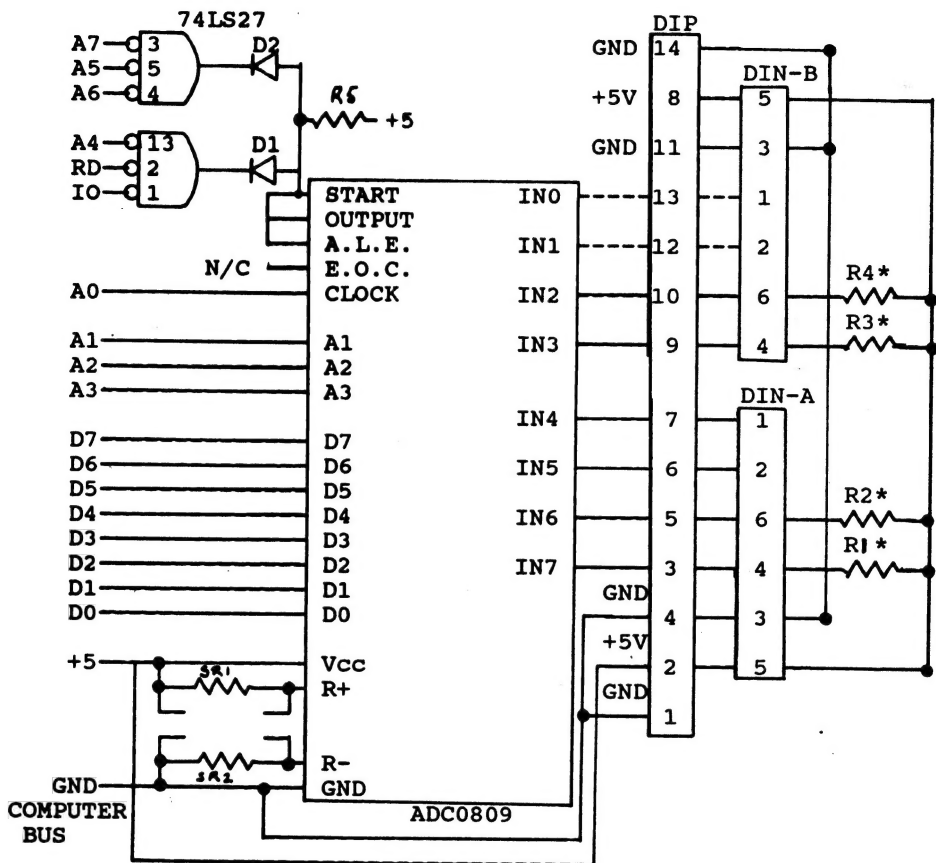
Copyright (C) 1986
Zebra Systems, Inc
78-06 Jamaica Ave.
Woodhaven, NY 11421

Theory of Operation

The ZAD plugs on to the expansion bus of your ZX81, TS1000, TS1500, or TS2068 computer. It is port addressed and can be read using the IN command on the TS2068 or with machine language drivers on all these computers. The ZAD is located at the even port addresses from 0 to 14. The odd addresses that use bit A0 were purposely not used so that there would be no conflict with the keyboard scanning hardware on the ZX81, TS1000, and TS1500 computers.

It takes about 2 milli-seconds for the ZAD to complete a single analog to digital conversion on a channel. To start a conversion cycle, you read the address location corresponding to the channel that you want to measure. Then you must delay at least 2 millisecond for the conversion to be completed properly. To get the results you then do an input from any of the ZAD's port addresses. This action will do two things: first it will give you the results of the recently completed conversion. Second it will start a new conversion on whichever channel you've just addressed to get this reading.

SCHEMATIC **ZEBRA A/D INTERFACE**



Note 1: Resistors R1 through R4 are only used where the ZAD is configured as a Zebra Graphics Interface. In that configuration, the resistors serve as pull-ups for the graphics tablet buttons.

Note 2: Resistors SR1 and SR2 are scaling resistors. They appear on all configurations but are shorted out except in the Zebra Graphics Interface configuration. Their purpose is to offset the measurement voltage range slightly away from both power supplies, (approximately 0.1 volt to 4.9 volt,) instead of the usual 0-5 volts. This enables full scale 0-255 range of readings even though the Zebra Graphics Tablet has some residual resistance along its edges.

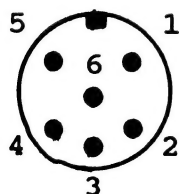
Zebra A/D Interface

Connector Signal Assignments

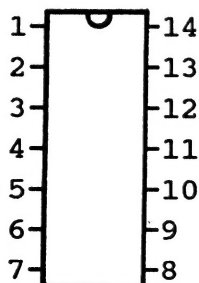
D.I.N. Connector Pin Number	DIP SOCKET PIN NO.	SIGNAL	ADDRESS PORT
A1	7	INPUT 4	8
A2	6	INPUT 5	10
A3	4	GND	
A4	3	INPUT 7	14
A5	2	+5V	
A6	5	INPUT 6	12
--	1	GND	
--	14	GND	
B1	13	INPUT 0	0
B2	12	INPUT 1	2
B3	11	GND	
B4	9	INPUT 3	6
B5	8	+5V	
B6	10	INPUT 2	4

D.I.N. PIN-OUT

DIP PIN-OUT



A and B DIN CONNECTORS



Sample BASIC Driver

Below is an example of how to read the ZAD from TS2068 BASIC:

```
10 PRINT "ENTER A CHANNEL # TO READ (1-8)
20 INPUT X
30 IF X < 1 OR X > 8 THEN GOTO 10
35 REM CALC. INPUT PORT NUMBER
40 LET CH=(X-1)*2
45 REM START CONVERSION OF CHANNEL CH
50 LET Y=IN CH
55 REM GET RESULTS OF LAST CONVERSION
60 LET Y=IN CH
70 PRINT "AT INPUT";X;"VOLTAGE= ";
80 PRINT (Y*5/256); "VOLTS."
90 GOTO 10
```

Here is a shorter program to keep reading a single port:

```
10 LET V=INPUT 0
20 PRINT "THE VOLTAGE ON CHANNEL 1 IS";V
30 GOTO 10
```

SAMPLE MACHINE CODE DRIVER

(Reads all 8 channels)

The following is a relocatable machine language driver for the ZAD. It can be poked into memory at any safe location and called via a USR call function. The data returned is contained in an eight byte buffer exactly 46 bytes after the first address of this routine.

0000	ED4B8640	00100	LD	BC, (16518)
0004	11E1E9	00110	LD	DE, 0E9E1H
0007	ED538640	00120	LD	(16518), DE
000B	CD8640	00130	CALL	16518
000E	ED438640	00140	LD	(16518), BC
0012	AF	00150	XOR	A
0013	3C	00155	INC	A
0014	111F00	00160	LD	DE, DATA-RET
0017	19	00170	ADD	HL, DE
0018	0609	00180	LD	B, 9
001A	4F	00190	LD	C, A
001B	ED78	00200	IN	A, (C)
001D	C5	00210	PUSH	BC
001E	067F	00217	LD	B, 127
0020	10FE	00223	DJNZ	DELAY
0022	C1	00230	POP	BC
0023	77	00240	LD	(HL), A
0024	23	00250	INC	HL
0025	79	00260	LD	A, C
0026	3C	00270	INC	A
0027	3C	00280	INC	A
0028	E60F	00290	AND	15
002A	10EE	00300	DJNZ	LOOP
002C	C9	00310	RET	
002D	30	00320	DATA	'012345678'

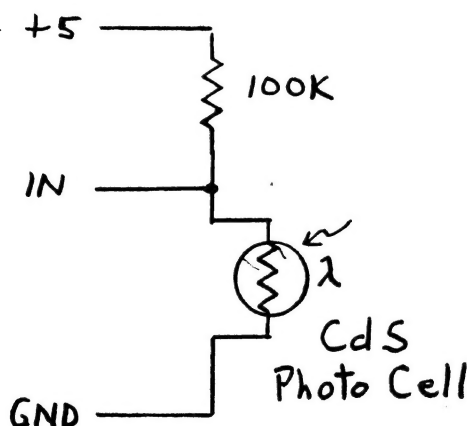
Decimal Listing of Preceding Routine

16514	237	16515	75	16516	134
16517	64	16518	17	16519	225
16520	230	16521	237	16522	83
16523	134	16524	64	16525	205
16526	134	16527	64	16528	237
16529	67	16530	134	16531	64
16532	175	16533	60	16534	17
16535	31	16536	0	16537	25
16538	6	16539	9	16540	79
16541	237	16542	120	16543	197
16544	6	16545	127	16546	16
16547	254	16548	193	16549	119
16550	35	16551	121	16552	60
16553	60	16554	230	16555	15
16556	16	16557	238	16558	201

Photocell Light-detector

Inexpensive Cadmium Sulfide photocells are easy to find and simple to use. The resistance of these cells is very high when they are in the dark. But when light hits them, their resistance falls dramatically. The exact resistance change versus light sensitivity depends upon the manufacturer and part number.

Zebra Systems used Cd/S in their light pen design and it was found that the cells are quite fast. Fast enough to repond to the peak light intensity as a CRT scanning beam passed by at 60 TV frames per second. The cells we tested also were more sensitive to red light than to blue.

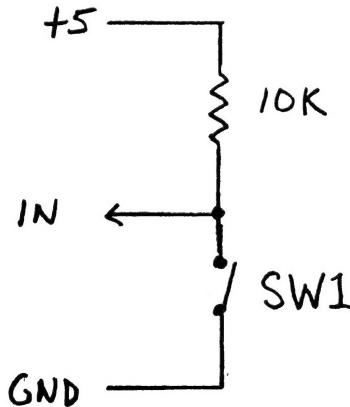


Switch Contact Monitoring

There are many applications for simple contact closure monitoring. The circuit below shows a single contact. A simple 10K pull-up resistor is used so that when the switch is opened, the voltage at the monitoring point will be near 5 volts; when the switch is closed the voltage will be near 0 volts. Your computer software can determine whether the contact is open or closed by simply comparing the voltage to 2.5 volts.

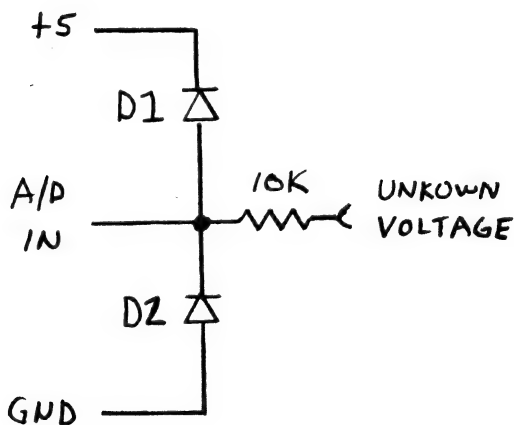
```
8 REM PUT INPUT RESULTS INTO
9 REM VARIABLE V1, THEN...
10 IF V1 > 127 THEN GOTO 50
20 PRINT "CONTACT IS CLOSED"
30 GOTO 50
40 PRINT "CONTACT IS OPEN"
50 CONTINUE
```

The contact could be a joystick fire button, alarm system window switch, control panel selector switch, or anything else.



Over Voltage Protection

The Zebra A/D has a 5 Volt DC full scale range, and is subject to damage if voltages outside this range are applied. The circuit below show one possible method for protecting the A/D. An input resistor and two diodes are used. Within the normal 0 to 5 Volt range the diodes will remain reverse biased. If the source voltage goes higher than +5 volts, then the diode D1 to the +5volt supply will conduct and limit the A/D input voltage to not much higher than the 5Volts. Similarly for negative voltages, diode D2 will prevent A/D input from going much below 0 Volts. The value of the input resistor R1 should be chosen judiciously to limit the current through it and the protection diodes under your worst-case input voltage.

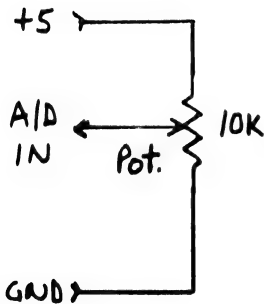


Potentiometer Inputs

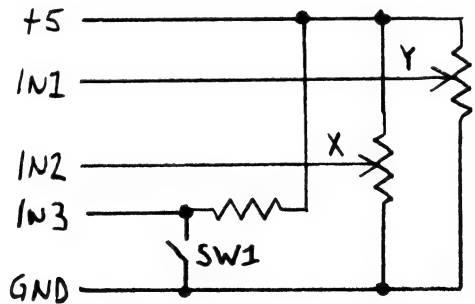
There are many types of potentiometers. Simple inexpensive ones are rotary and linear potentiometers consisting of a resistive ink on a substrate and a moving metallic wiper contact. For example, the volume control on virtually every TV or radio is a potentiometer. As shown in Figure 1, you can impress the ZAD's +5 volt power supply across the potentiometer and then monitor the voltage at the wiper. This voltage will vary with the wipers position.

A good potentiometer for use with the ZAD would be a 10K potentiometer with a wiper resistance that varies linearly with position. Potentiometers used as volume controls often vary logarithmically with position since the ear's sensitivity is logarithmic. If you use one of these pots, you will have lots of resolution at one end of its control and very little at the other.

Note that an analog joystick is merely a special application of two rotary potentiometers that have been mechanically coupled to a joystick handle. You can use one ZAD channel to monitor the X direction pot, one for the Y direction, and yet another for the fire button contact switch.



Potentiometer



Z Axis Joystick

D.C. Voltmeter

You can extend the positive voltage range of your ZAD by including a resistive divider circuit on its input. For example the network shown here in figure 1, will double the normal 5 volt input range to 10 volts full scale. Notice that we have included protection diodes. For best accuracy these diodes should be low leakage.

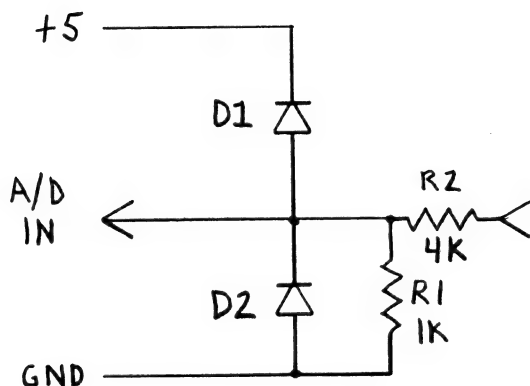


Figure 1.

this page intentionally left blank

ADC0808, ADC0809 8-Bit μ P Compatible A/D Converters With 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8 single-ended analog signals.

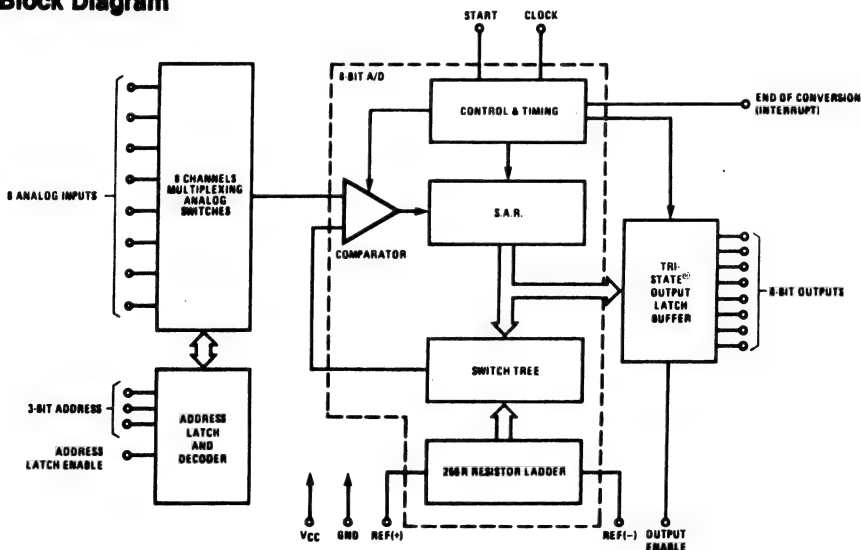
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE[®] outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet.

Features

- Resolution — 8-bits
- Total unadjusted error — $\pm 1/2$ LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μ s
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T²L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 28-pin DIP package
- Temperature range -40°C to +85°C or -55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE[®] output

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	8.5V
Voltage at Any Pin Except Control Inputs	-0.3V to ($V_{CC} + 0.3V$)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADP A, ADD B, ADD C)	-0.3V to +15V
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ\text{C}$	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} = T_A = T_{MAX}$ -55°C to $T_A = +125^\circ\text{C}$
ADC0808CJ, ADC0808CCN, ADC0809CCN	-40°C to $T_A = +85^\circ\text{C}$
Range of V_{CC} (Note 1)	4.5V to 5.5V

Electrical Characteristics

Converter Specifications: $V_{CC} = 5V_{DC} = V_{REF(+)}$, $V_{REF(-)} = \text{GND}$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640 \text{ kHz}$ unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
ADC0808					
Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			$\pm 1/2$ $\pm 3/4$	LSB LSB
ADC0809					
Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			± 1 $\pm 1 1/4$	LSB LSB
Input Resistance	From $\text{Ref}(+)$ to $\text{Ref}(-)$	1.0	2.5		k Ω
Analog Input Voltage Range	(Note 4) $V(+)$ or $V(-)$	GND-0.10		$V_{CC} + 0.10$	V_{DC}
$V_{REF(+)}$ Voltage, Top of Ladder	Measured at $\text{Ref}(+)$		V_{CC}	$V_{CC} + 0.1$	V
$\frac{V_{REF(+)} + V_{REF(-)}}{2}$ Voltage, Center of Ladder		$V_{CC}/2 - 0.1$	$V_{CC}/2$	$V_{CC}/2 + 0.1$	V
$V_{REF(-)}$ Voltage, Bottom of Ladder	Measured at $\text{Ref}(-)$	-0.1	0		V
Comparator Input Current	$f_c = 640 \text{ kHz}$, (Note 6)	-2	± 0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ $4.5V \leq V_{CC} \leq 5.5V$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ unless otherwise noted
ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \leq V_{CC} \leq 5.25V$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER					
$I_{OFF(+)}$ OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 5V$, $T_A = 25^\circ\text{C}$ T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$ OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 0$, $T_A = 25^\circ\text{C}$ T_{MIN} to T_{MAX}	-200 -1.0	-10		nA μA
CONTROL INPUTS					
$V_{IN(1)}$ Logical "1" Input Voltage		$V_{CC} - 1.5$			V
$V_{IN(0)}$ Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$ Logical "1" Input Current (The Control Inputs)	$V_{IN} = 15V$			1.0	μA
$I_{IN(0)}$ Logical "0" Input Current (The Control Inputs)	$V_{IN} = 0$	-1.0			μA
I_{CC} Supply Current	$f_{CLK} = 640 \text{ kHz}$		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ 4.5V $\leq V_{CC} \leq 5.5V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ unless otherwise noted
ADC0808CCJ, ADC0808CCN, and ADC0809CCN 4.75 $\leq V_{CC} \leq 5.25V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)					
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360 \mu A$	$V_{CC}-0.4$		V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6 \text{ mA}$		0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2 \text{ mA}$		0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O = 5V$ $V_O = 0$	-3	3	μA μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_1 = t_f = 20 \text{ ns}$ and $T_A = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(Figure 5)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(Figure 5)		100	200	ns
t_s	Minimum Address Set-Up Time	(Figure 5)		25	50	ns
t_H	Minimum Address Hold Time	(Figure 5)		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ (Figure 5)		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50 \text{ pF}$, $R_L = 10k$ (Figure 8)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10 \text{ pF}$, $R_L = 10k$ (Figure 8)		125	250	ns
t_c	Conversion Time	$f_c = 640 \text{ kHz}$, (Figure 5) (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(Figure 5)	0		$8 + 2 \mu s$	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE [®] Output Capacitance	At TRI-STATE [®] Outputs, (Note 12)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See Figure 3. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See Figure 13.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (Figure 6). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed

to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (Figure 1) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in Figure 1 are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached $+1/2$ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n -iterations are required for an n -bit converter. Figure 2 shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

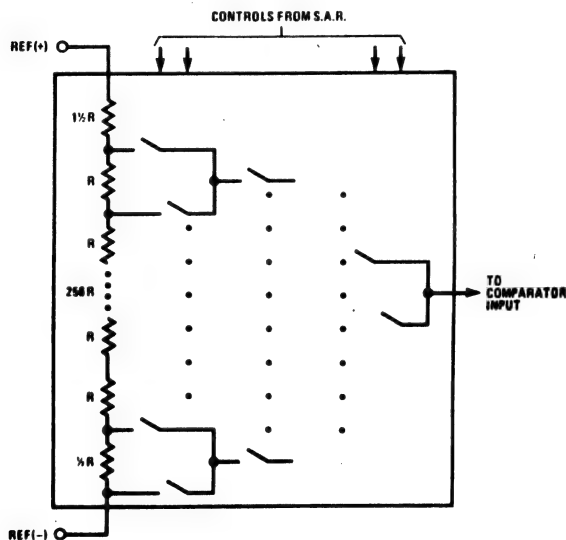


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the

comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

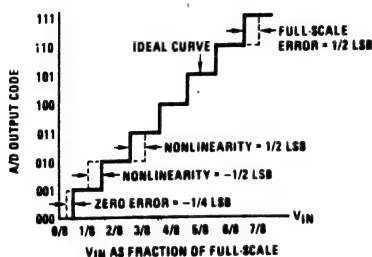


FIGURE 2. 3-Bit A/D Transfer Curve

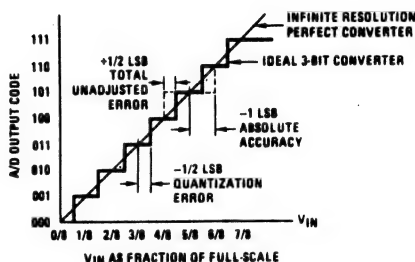


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

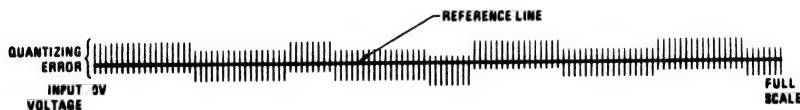
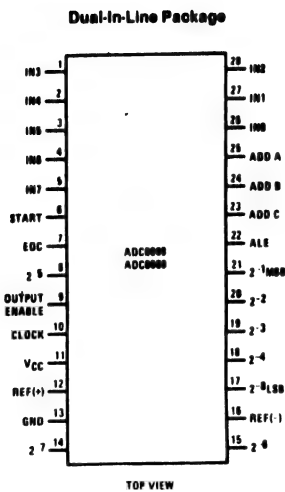


FIGURE 4. Typical Error Curve

Connection Diagram



Timing Diagram

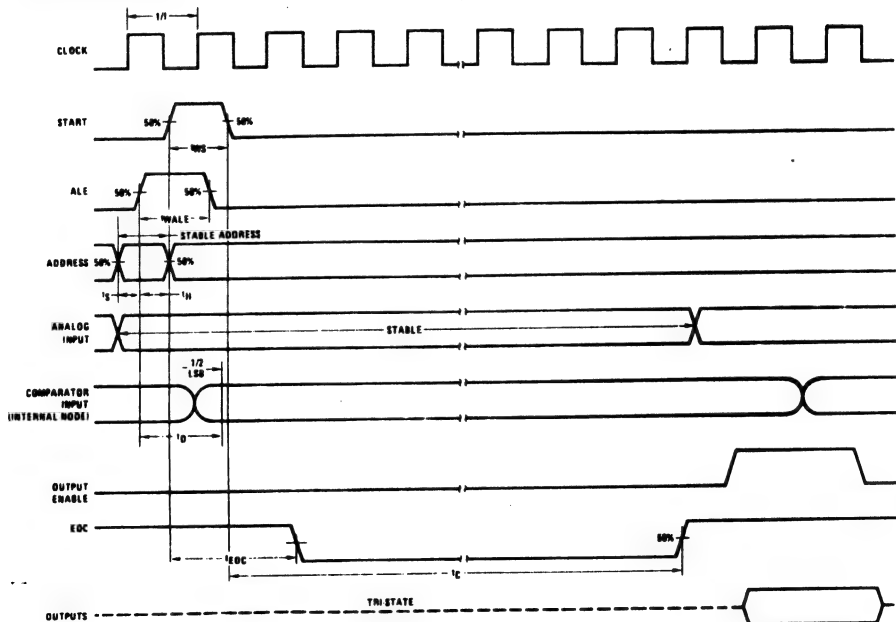


FIGURE 5

Typical Performance Characteristics

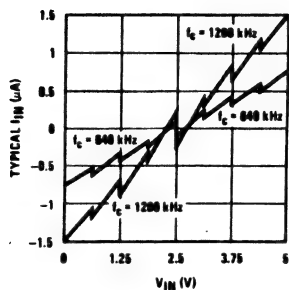


FIGURE 6. Comparator I_{IN} vs V_{IN}
($V_{CC} = V_{REF} = 5V$)

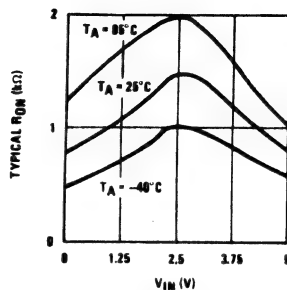


FIGURE 7. Multiplexer R_{ON} vs V_{IN}
($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

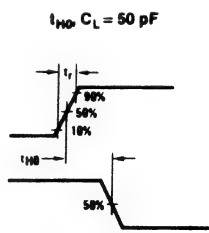
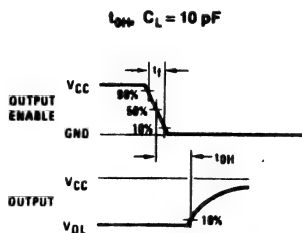
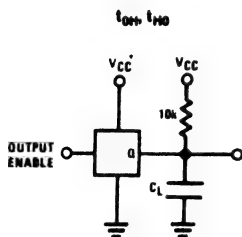
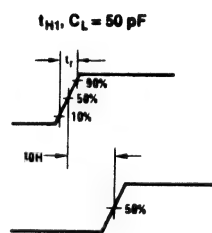
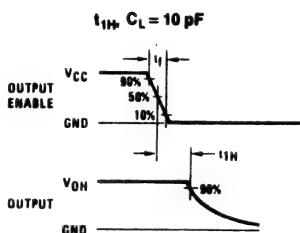
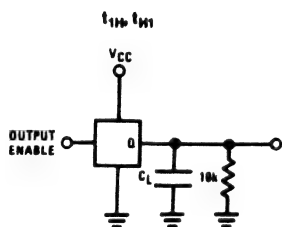


FIGURE 8

Applications Information

OPERATION

1.0 Ratimetric Conversion

The ADC0806, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratimetric conversion systems. In ratimetric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0806 is expressed by the equation

$$\frac{V_{IN} - V_Z}{V_{FS} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0806

V_{FS} = Full-scale voltage

V_Z = Zero voltage

D_X = Data point being measured

D_{MAX} = Maximum data limit

D_{MIN} = Minimum data limit

A good example of a ratimetric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0806, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (Figure 9).

Ratimetric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(-), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratimetric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

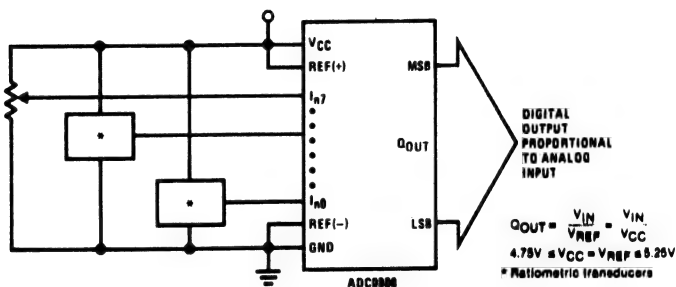


FIGURE 9. Ratimetric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In Figure 11 a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in Figure 12. The LM301 is overcompensated to insure stability when loaded by the $10\ \mu\text{F}$ output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In Figure 13, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

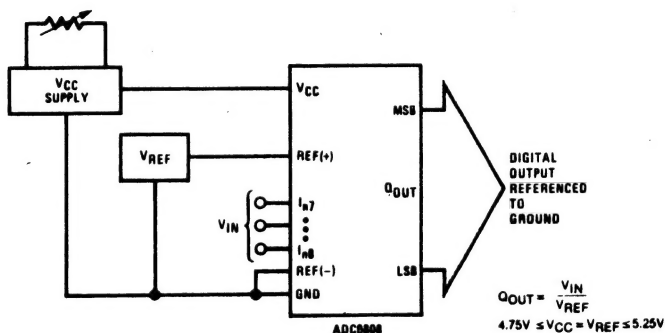


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

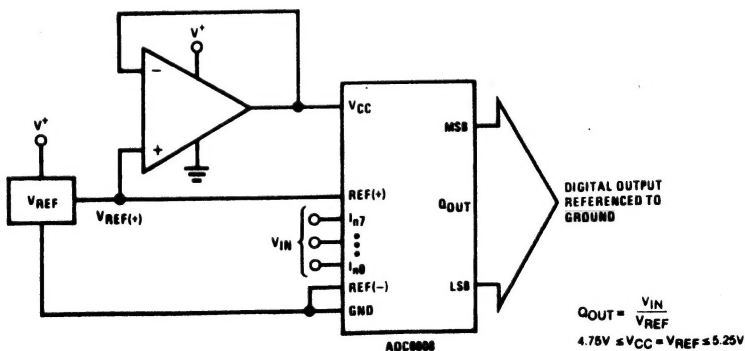


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

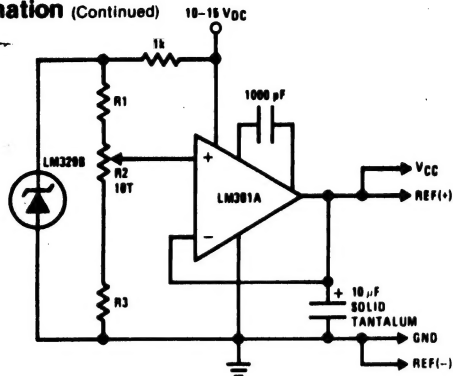


FIGURE 12. Typical Reference and Supply Circuit

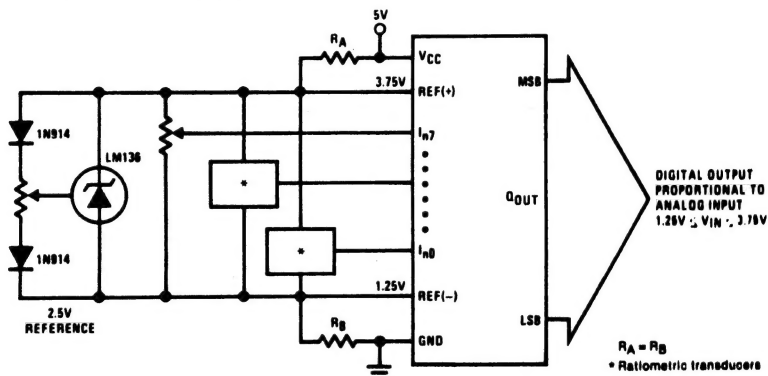


FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and $N+1$ is given by:

$$V_{IN} = \left[(V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right] + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left[(V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right] + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input

$V_{REF(+)}$ = Voltage at Ref(+)

$V_{REF(-)}$ = Voltage at Ref(-)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} + 512$)

4.0 Analog Comparator Inputs

The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in Figure 6.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

*** NOTES ***

This image shows a single sheet of white paper with horizontal blue or grey ruling lines. The lines are evenly spaced and run across the width of the page. There is no handwriting or other markings on the paper.

